CLAIMS

1. In an analog-to-digital converter having a plurality of stages arranged in pipeline, a method of performing a digital dither to provide a digital output signal, the method comprising acts of:

generating a plurality of digital output bits from samples of an analog input signal, the plurality of digital output bits having associated bit weights including an LSB bit weight;

generating at least one random bit having a sub-LSB bit weight;

providing a plurality of calibration bits, at least one of the plurality of calibration bits having a sub-LSB bit weight; and

applying the calibration bits to the plurality of digital output bits and at least one random bit to form the digital output signal.

2. The method of claim 1, wherein the act of applying the calibration bits includes an act of adding the plurality of digital output bits, the at least one random bit and the plurality of calibration bits according to bit weight.

3. The method of claim 1, wherein the act of generating at least one random bit includes an act of generating a plurality of random bits having sub-LSB bit weights.

4. The method of claim 3, wherein the act of generating a plurality of random bits includes an act of generating a first random bit having at least a resolution of 1/2 LSB and a second random bit having a resolution of at least 1/4 LSB.

5. The method of claim 3, wherein the act of randomly generating a plurality of random bits includes an act of generating a first random bit having a resolution of at least 1/8 LSB and a second random bit having a resolution of at least 1/16 LSB.

6. The method of claim 1, wherein the act of generating a plurality of digital output bits includes an act of generating at least one digital output bit having a sub-LSB bit weight.

7. The method of claim 6, wherein the act of generating at least one digital output bit having a sub-LSB bit weight includes generating at least a first digital output bit having a resolution of at least 1/2 LSB and at least a second digital output bit having a resolution of at least 1/4 LSB.

8. The method of claim 7, wherein the act of generating at least one random bit includes an act of generating a plurality of random bits including at least a first random bit having a resolution of at least 1/8 LSB and a second random bit having a resolution of at least 1/16 LSB.

9. The method of claim 1, wherein the act of generating at least one random bit includes shifting the at least one random bit from a linear feedback shift register (LFSR).

10. The method of claim 9, wherein the act of shifting at least one random bit from a linear feedback shift register includes an act of shifting the at least one random bit from an LFSR configured to produce a maximal length sequence.

11. An analog-to-digital converter (ADC) for providing a digital output signal indicative of an analog input signal, the ADC comprising:

a plurality of stages arranged in a pipeline, each of the plurality of stages providing at least one bit from samples of the analog input signal to form a plurality of digital output bits, at least one of the plurality of digital output bits having an LSB bit weight;

a random bit generator adapted to generate at least one random bit having a sub-LSB bit weight;

at least one register adapted to store a plurality of calibration bits, at least one of the plurality of calibration bits having a sub-LSB bit weight; and

a correction component arranged to receive at least some of the plurality of digital output bits, the plurality of calibration bits and the at least one random bit, the correction component configured to modify the plurality of digital output bits according to the calibration bits and the at least one random bit to form the digital output signal.

12. The ADC of claim 6, wherein at least one of the plurality of stages provides at least one bit having a sub-LSB bit weight.

13. The ADC of claim 12, wherein the plurality of digital output bits provided by the plurality of stages include a first bit having a bit weight of 1/2 LSB and a second bit having a bit weight of 1/4 LSB.

14. The ADC of claim 13, wherein the random number generator is adapted to generate a plurality of random bits including a first random bit having a bit weight of 1/8 LSB and a second random bit having a bit weight of 1/16 LSB.

15. The ADC of claim 11, wherein the random number generator is adapted to generate a plurality of random bits including a first random bit having a resolution of at least ½ LSB and a second random bit having a resolution of at least ¼ LSB.

16. The ADC of claim 11, wherein the random number generator is adapted to generate a plurality of random bits including a first random bit having a resolution of at least 1/8 LSB and a second random bit having a resolution of at least 1/16 LSB.

17. The ADC of claim 11, wherein the random number generator includes a linear feedback shift register (LFSR).

18. The ADC of claim 17, wherein the LFSR is configured to generate maximal length sequences.

19. A digital signal generated by a pipeline ADC and representing samples of an analog input signal, the digital signal comprising:

M bits having associated bit weights 2^{M-1} through 2^0, respectively, wherein a value of at least a bit having associated bit weight 2^0 is determined by adding together digital output bits provided by the pipeline, a plurality of calibration bits having at least one bit with a sub-LSB bit weight, and at least one random bit having a sub-LSB bit weight.